

Completing SOCKs

ECE 686 Top Down SOC Design
Project Presentation

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Dec 13, 2006

Existing SOCKs from OSU

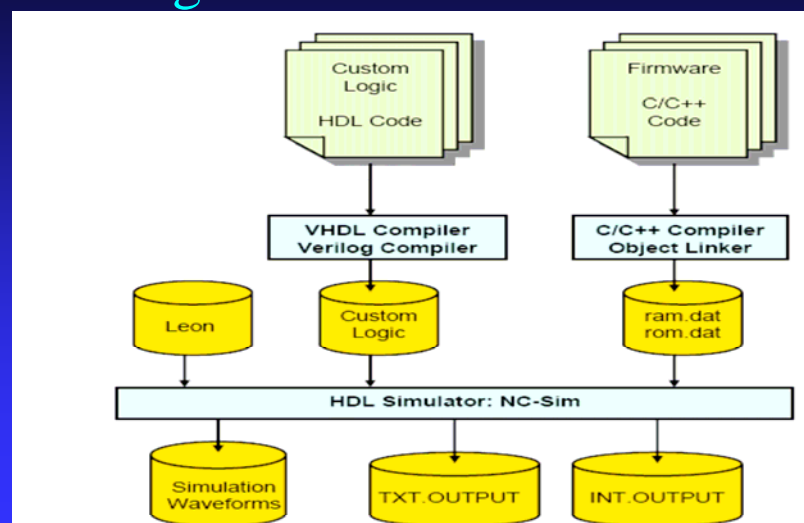


Fig from 'Socks_slides.pdf' on OSU website

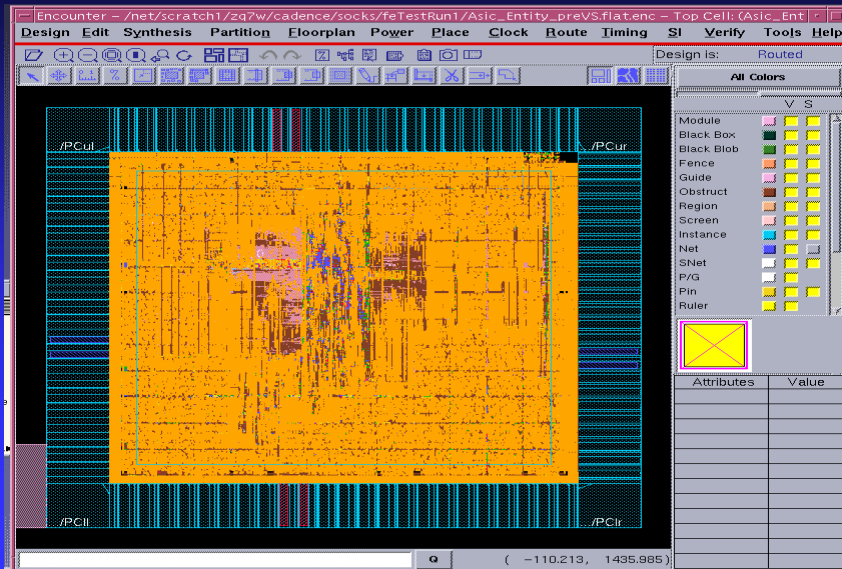
Missing Features of OSU Flow

- Frontend – logic synthesis
- Backend – placement and route
 - ◆ Pads
 - ◆ Memory
- Design for Test
 - ◆ Scan chain
 - ◆ BIST

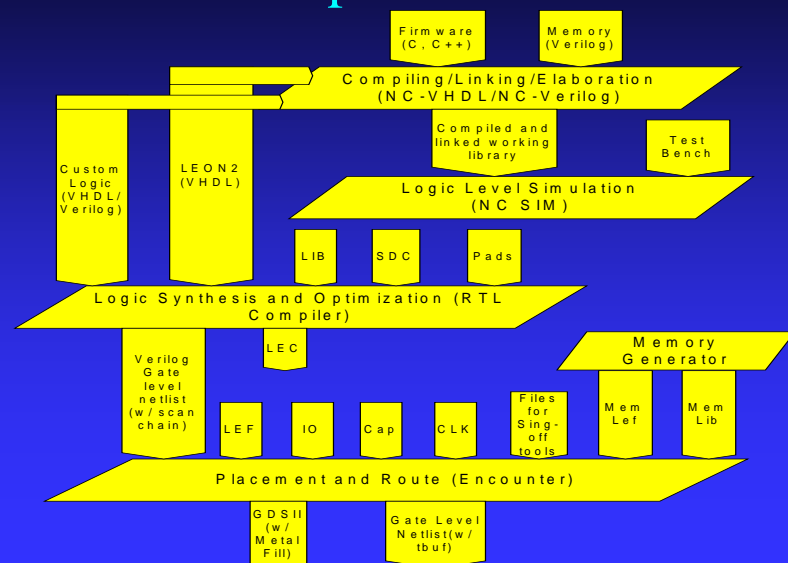
Implementation

- Implementation Flows
 - ◆ Low power flow
 - ◆ Hierarchical flow
 - ◆ Flat flow
- Difference from ‘Mickey Mouse’

Final Look



A More Complete Flow



Deliverables and Conclusion

- Completing the SOCKs flow
- Migrated memory generator
- Mickey Mouse[®] VS *Donald Duck*[®] (?)
- Automation VS Interference
- Implementation issues

Discussion and Future Work

- Other flows
- Power and timing
- DFT
- Verification
- HW-SW Co-design
- Technology migration